ABSTRACT

A semiconductor package is disclosed that comprises a chip paddle and a semiconductor chip that has a plurality of bond pads. The semiconductor chip is located on an upper surface of the chip paddle. Internal leads are formed at intervals along a circumference of the chip paddle. The internal leads are in electrical communication with the bond pads. The semiconductor chip, the chip paddle and the internal leads are encapsulated by an encapsulation material. The height of the semiconductor package of the invention is minimized by half etching the chip paddle to reduce the thickness of the chip paddle such that the thickness of the chip paddle is less than the thickness of the internal leads. Preferably, the chip paddle of the invention is about 25-75 % of the thickness of the internal leads.